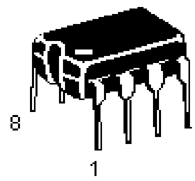
General Description

The HWD63020Dx is a monolithic step-down (buck) regulator with a built in internal Power MOSFET. It achieves 2A continuous output current over a wide input supply range with excellent load and line regulation.
Current mode operation provides fast transient response and eases loop stabilization.
Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws less than 20uA current.
The HWD63020Dx requires a minimum number of readily available standard external components. A synchronization pin allows the part to be driven to 600KHz.

Features

- 2A Output Current
- 0.18Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic capacitors
- Up to 95% Efficiency
- Less than 8uA Shutdown Mode
- Fixed 360kHz frequency
- Thermal Shutdown
- Cycle-by-cycle over current protection
- Wide 4.75V to 12V operating input range
- Output Adjustable from 1.22 to 0.85Vin
- Programmable under voltage lockout
- Frequency Synchronization Input
- Available in 8 pin DIP AND SOP packages



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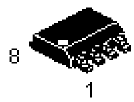

SO8

PLASTIC PACKAGE

Applications

- DVD, Car Electronics, GPS
- Distributed Power Systems
- Communication Productions
- Efficient Pre-Regulator for Linear Regulators
- Computer (Lan Card, Modem, Monitor, Mother Board, Sound Card…)
- Battery Charger，Phone, Databank, Toys, LED Display, Satellite Receiver…

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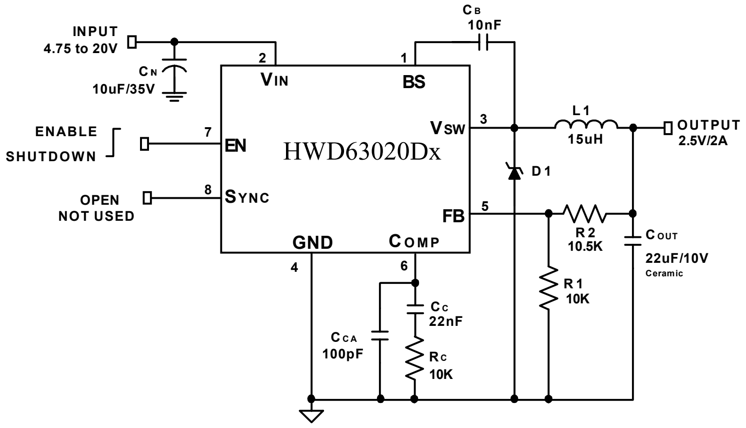
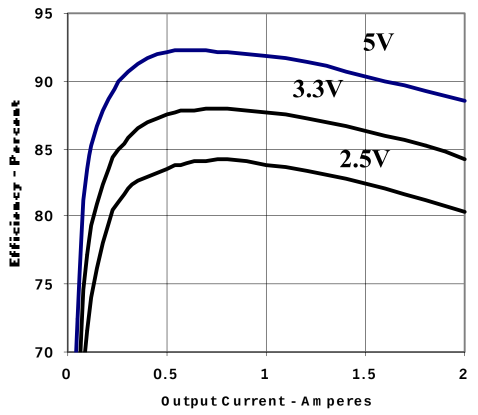
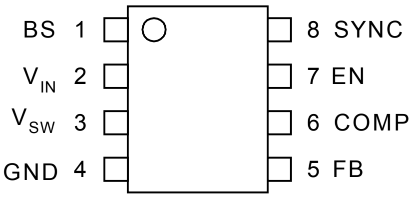
Typical Application Circuit



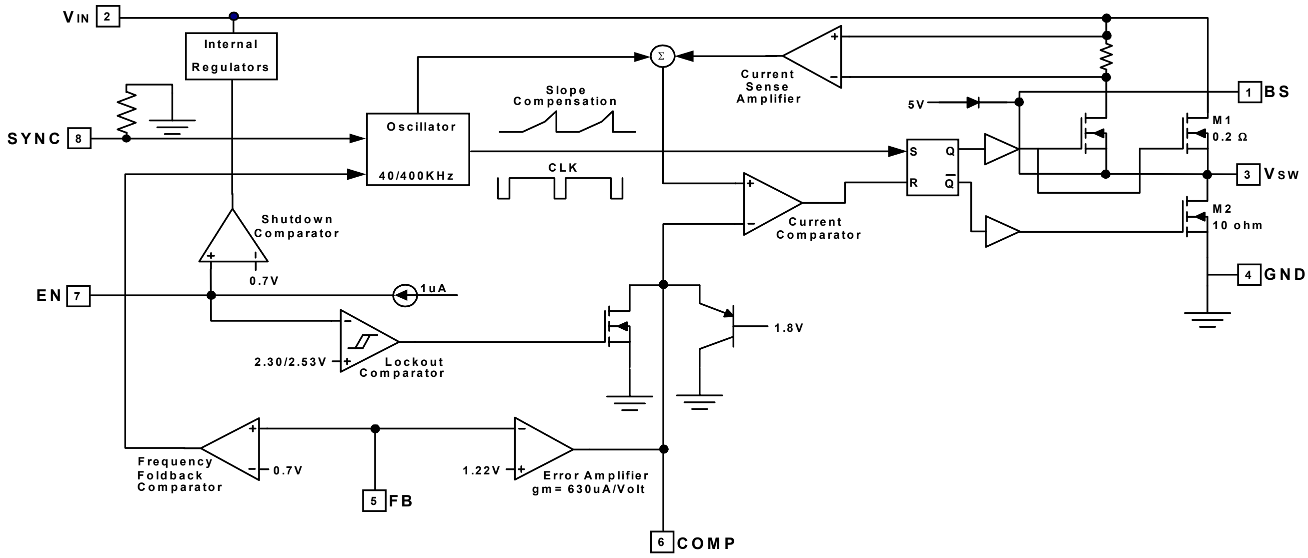
Efficiency versus Output Current and Voltage. V_{IN}=10V





Functional Block Diagram

HWD63020Dx BLOCK DIAGRAM



Functional Description

The HWD63020Dx is a current mode regulator. That is, the compensation pin voltage is proportional to the current delivered to the load.

At the beginning of a cycle: the upper transistor M1 is off; the lower transistor M2 on; the V_C pin voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 400KHz CLK signal sets the RS Flip-Flop. Its output turns off M2 and turns on M1 thus connecting the Switch pin and inductor to the Input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the error amplifier output by the Current Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the Comp pin voltage, the RS Flip-Flop is reset and the chip reverts to its initial M1 off, M2 on state. If the Current Sense Amplifier plus Slope Compensation signal does not exceed the V_C voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error amplifier integrates the voltage difference between the feedback and the 1.22V bandgap reference. The polarity is such that feedback pin voltages lower than 1.22V increases the V_C pin voltage. Since the V_C pin's voltage is proportional to the peak inductor current an increase in its voltage increases current delivered to the output.

The lower 10Ω switch ensures that the bootstrap capacitor voltage is charged during light load conditions. External Schottky Diode D1 carries most of the inductor current.

Absolute Maximum Ratings (Note 1)

Supply Voltage (Vin) ------------------------------- 15V
Switch Voltage ------------------------------------- -1V to Vin +1V
Boost Voltage --------------------------------------- V_{SW} + 6V
Feedback Voltage ---------------------------------- –0.3 to 6V
Enable/UVLO Voltage ----------------------------- –0.3 to 6V
V_C Voltage -- –0.3 to 6V
Sync Voltage -- –0.3 to 6V
Junction Temperature ----------------------------- 150°C
Lead Temperature ---------------------------------- 260°C
Storage Temperature ------------------------------- -65°C to 150°C

Recommended Operating Conditions (Note 2)

Input Voltage Vcc ---------------------------------- 4.75V to 15V
Operating Temperature ---------------------------- -40°C to +125°C

ESD Susceptibility

(Human Model) ------------------------------------- 2kV

Package Thermal Characteristics

$R\Theta_{JA}$ (8 pin SOIC) ---------------------------------- 160°C/W
$R\Theta_{JA}$ (8 pin PDIP) ---------------------------------- 105°C/W

Electrical Characteristics

(Unless otherwise specified V_{IN}=12V, T_A=25 °C)

Parameters	Condition	Min	Typ	Max	Units
Feedback Voltage	4.75V ≤ VIN ≤ 15V Comp < 2V	1.198	1.222	1.246	V
Upper Switch On Resistance			0.18		Ohms
Lower Switch On Resistance			10		Ohms
Upper Switch Leakage	EN=0V; VSW=0V		0	10	uA
Current Limit		2.4	2.85	3.3	A
Current Limit Gain. Output Current to Comp Pin Voltage			1.95		A/V
Error Amplifier Voltage Gain			400		V/V
Error Amplifier Transconductance	ΔIC = ±10 uA	500	770	1100	μMho
Oscillator Frequency		342	360	380	KHz
Short Circuit Frequency	FB = 0V	30	42	54	KHz
Sync Frequency	Sync Drive 0 to 2.7V			600	KHz
Maximum Duty Cycle	FB = 1.0V		95		%
Minimum Duty Cycle	FB = 1.5V			0	%
Enable Threshold	ICC > 100uA	0.7	1.0	1.3	V
Enable Pull Up Current	EN = 0V	1.15	1.46	1.8	uA
Under Voltage Lockout Threshold High Going		2.37	2.495	2.62	V
Under Voltage Lockout Threshold Hysteresis			210		mV
Supply current (quiescent)	EN ≤ 0.4V		23	36	uA
Supply current (operating)	EN ≥ 2.6V; VFB =1.4V		1.0	1.2	mA
Thermal Shutdown			160		C

Note 1. Exceeding these ratings may damage the device.
Note 2. The device is not guaranteed to function outside its operating rating.
Note 3. Measured on approximately 1” square of 1 oz. copper surrounding device leads.

Pin Functions

BS (Pin 1) Bootstrap

This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between V_{SW} and Bootstrap pins to effect a floating supply across the power switch driver. The voltage across C_B is about 5V and is supplied by the internal +5V supply when the V_{SW} pin voltage is low.

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V_{IN} (Pin 2) Supply Voltage

The HWD63020Dx operates from a +4.75 to +12V unregulated input. Cin isne eded to prevent large voltage spikes from appearing at the input.

V_{SW} (Pin 3) Switch

This connects the inductor to either the V_{IN} through M1 or to GND through M2.

GND (Pin 4) Ground

This pin is the voltage reference for the regulated voltage. For this reason care must be taken in its layout. This node should be placed outside of the D_{SCH} to C_{IN} ground loop to prevent switching current spikes to induce voltage noise into the part.

FB (Pin 5) Feedback

An external resistor divider from the output voltage to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillation frequency when the FB voltage is below 650mV

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COMP (Pin 6) Compensation

This node is the output of the transconductance amplifier error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensation section for exact details.

EN (Pin 7) Enable/UVLO

A voltage greater than 2.45V enables operation. Leave the input unconnected if unused. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from Vin to GND. For complete low current shutdown its needs to be less than 0.7V.

SYNC (Pin 8) Synchronization Input

This pin is used to synchronize the internal oscillator frequency to an external source. A high going signal greater than 2V resets the oscillator and will connect V_{SW} from V_{IN} to GND if it is not already in this state. The V_{SW} pin will make a high transition approximately 350ns after a rising edge Sync signal. The frequency of the external Sync signal needs to be greater than 440 kHz. Leave the input unconnected if unused.

Applications Information

Bootstrap Capacitor – CB
This bypasses the upper switch gate drive. Its value should be $\geq$ 4.7nF. For simplicity of design this capacitor can be the same value as Compensation cap C_C.

Compensation Capacitor – CC
This is the system compensation cap that is in series with RC. Using a ceramic 10nF, 50V, X7R capacitor allows it to match CB.

Auxiliary Compensation Capacitor – CCA
This is the system compensation cap that connects between the VC and GND pin. This capacitor rolls off the high frequency noise and gain that can cause duty cycle jitter. On well laid out boards using low ESR Output capacitor (COUT) CCA may not be necessary. It –3DB frequency is set by 1 / 2π(RC X CCA). For RC=10Kohm and CCA=100pF the cut-off frequency is 159KHz which filters out the 400KHz switching noise and yet is above the GBW target of 10KHz to 80KHz Use a ceramic 100pF, 50V, X7 capacitor.

Compensation Resistor – RC
The loop compensation gain is directly proportional to RC's value. The higher its value the higher the gain. Calculation of its value is discussed in detail in the Loop Compensation section. Refer Table IV for recommended values that accompany a surface mount ceramic and special polymer output capacitor.

Feedback Divider Resistors – R2, R1
The Output voltage is set by R2 and R3:

VOUT = 1.22V[1 + (R2 / R1)]

The maximum recommended value of R1 is 100KΩ. Too high an impedance can make the Feedback node prone to noise injection particularly if unshielded inductors are used. 10KΩ is a good standard value.

Input Bypass Capacitor – CIN
CIN is the bulk supply capacitor whose value should be ≥ 10uF. The capacitor can be electrolytic, tantalum or ceramic. However since it absorbs the input switching current it requires an adequate ripple current rating. Its RMS current rating should be greater than approximately 1/2 of the output current.

For insuring stable operation CIN should be placed as close to the IC as possible. Alternately a smaller high quality ceramic 0.1uF capacitor may be placed closer to the IC and the bulk CIN placed further away. However if using this technique some caution is needed if the bulk CIN is also a high quality ceramic capacitor. Large voltage excursions caused by resonant energy oscillation between the two is possible.

Schottky Catch Diode – D1
D1 supplies most of the current to inductor L1 when VSW is low. The lower the forward Schottky voltage drop(VSCH) the higher the regulator efficiency.

Tables II provides the Schottky part numbers based on the maximum input voltage and current rating. Table III lists manufacturer's websites.

D1's maximum reverse voltage rating should be greater than the maximum input voltage VIN(Max).

The diode's average current rating must be above the average load current:

IDIODE(AVG) = ILOAD X [VIN – (VOUT+VSCH)] /VIN

Table II. Diode Selection Guide

V_{IN} (Max)	1A Diodes	2A Diodes
10V	10BQ15	30BQ15
12V	1N5817 B120 SS12	B220 SK23 SR22
15V	1N5818 B130 MBRS130 SS13	20BQ030 B230 SK23 SR23 SS23

Table III. Schottky Diode Manufacturers

Diodes, Inc.	www.diodes.com
Fairchild Semiconductor	www.fairchildsemi.com
General Semiconductor	www.gensemi.com
International Rectifier	www.irf.com
On Semiconductor	www.onsemi.com
Pan Jit International	www.panjit.com.tw

Inductor – L1

Optimal inductor selection involves trade-offs in electrical value, current rating and mechanical sizing.

Table IV lists the recommended minimum inductor values for common output voltage values. Table V Selection guide lists inductors by manufacturer, electrical value, maximum output current, DC resistance, core type, core material and mechanical sizing.

The Maximum current rating of the inductor should be above the peak operating current:

IPEAK = ILOAD + (VOUT)(VIN-VOUT)
2(L)(F)(VIN)

Example: VIN=12V Vout=3.3V, L=15uH, ILOAD=1.2A

IPEAK = 1.6 + (3.3)(12-3.3)
2(15u)(380KHz)(12)

IPEAK = 1.809A

Using Table V select a 15uH inductor with a Max IDC rating of > 1.809A.

Output Capacitor - COUT

The selection of the output capacitor is the most critical component of a switching regulator. Its electrical value and equivalent series resistance(ESR) directly affect:

- System stability
- Loop compensation components R_C and C_C
- Output ripple voltage

Moreover C_{OUT} is frequently the most expensive component of a switching regulator.

Figures 1 and 2 along with Table IV are schematics for two C_{OUT} components that have low ESR values.

Table IV. Recommended components for standard output voltages.

Vout	R2	L1 minimum
1.22V	0 K	6.8uH
1.5V	2.32K	6.8uH
1.8V	4.75 KΩ	10uH
2.5V	10.5 KΩ	10 uH
3.3V	16.9 KΩ	15 uH
5.0V	30.9 KΩ	22 uH

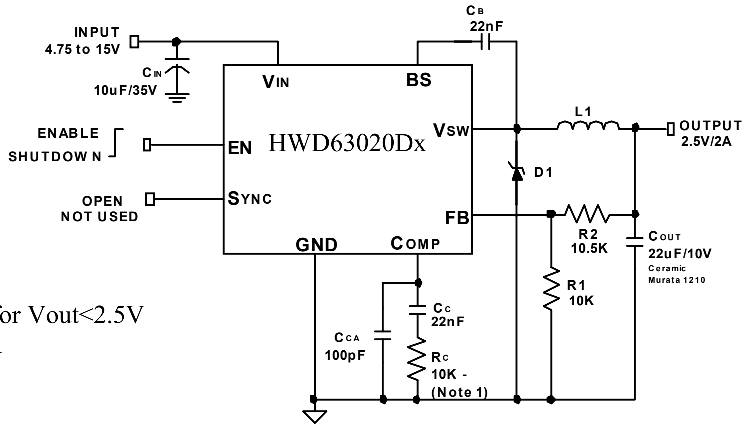


Figure 1. HWD63020Dx withMurata 22uF/10V Ceramic Output Capacitor.

Note 1 – for Vout<2.5V
R_C = 4.7K

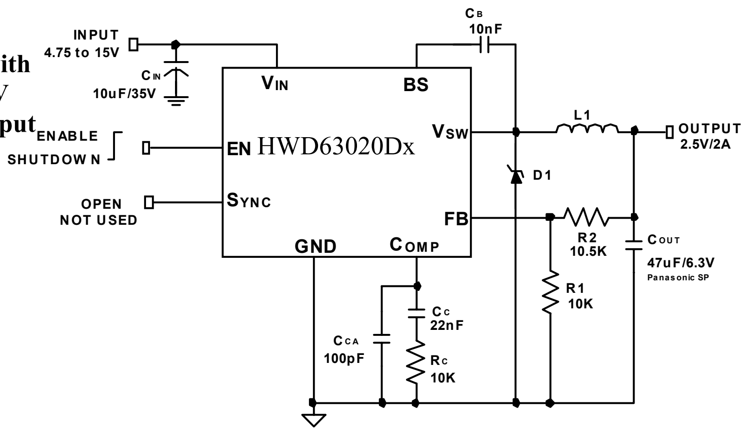


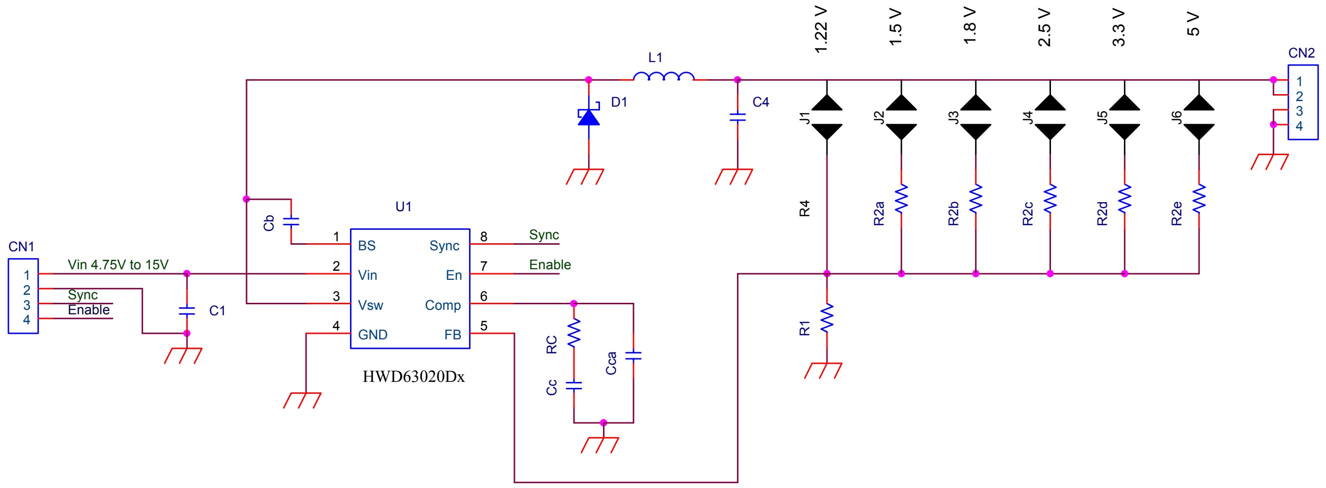
Figure 2. HWD63020Dx with Panasonic 47uF/6.3V Special PolymerOutput Capacitor.

Table V. Inductor Selection Guide

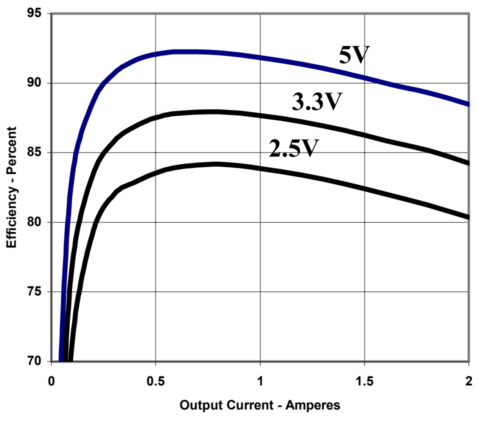
Vendor/Model	Value (uH)	Max I_{DC} (A)	Max DCR (Ω)	Core Type	Core Material	Package Dimensions (mm) W	L	H
Sumida								
CR75	10	2.3	0.070	Open	Ferrite	7.0	7.8	5.5
CR75	15	1.8	0.090	Open	Ferrite	7.0	7.8	5.5
CR75	22	1.5	0.110	Open	Ferrite	7.0	7.8	5.5
CDH74	10	2.75	0.056	Open	Ferrite	7.3	8.0	5.2
CDH74	15	2.1	0.083	Open	Ferrite	7.3	8.0	5.2
CDH74	22	1.7	0.130	Open	Ferrite	7.3	8.0	5.2
CDRH5D28	6.8	1.6	0.053	Shielded	Ferrite	5.5	5.7	5.5
CDRH5D28	10	1.3	0.065	Shielded	Ferrite	5.5	5.7	5.5
CDRH5D28	15	1.1	0.103	Shielded	Ferrite	5.5	5.7	5.5
CDRH6D28	6.8	2.3	0.031	Shielded	Ferrite	6.7	6.7	3.0
CDRH6D28	10	1.7	0.065	Shielded	Ferrite	6.7	6.7	3.0
CDRH6D28	15	1.6	0.057	Shielded	Ferrite	6.7	6.7	3.0
CDRH6D28	22	1.3	0.096	Shielded	Ferrite	6.7	6.7	3.0
CDRH6D38	6.8	2.3	0.031	Shielded	Ferrite	6.7	6.7	4.0
CDRH6D38	10	2.0	0.038	Shielded	Ferrite	6.7	6.7	4.0
CDRH6D38	15	1.6	0.057	Shielded	Ferrite	6.7	6.7	4.0
CDRH6D38	22	1.3	0.096	Shielded	Ferrite	6.7	6.7	4.0
CDRH104R	6.8	4.8	0.027	Shielded	Ferrite	10.1	10.0	3.0
CDRH104R	10	4.4	0.035	Shielded	Ferrite	10.1	10.0	3.0
CDRH104R	15	3.6	0.050	Shielded	Ferrite	10.1	10.0	3.0
CDRH104R	22	2.9	0.073	Shielded	Ferrite	10.1	10.0	3.0
Toko								
D53LC Type A	6.8	2.01	0.068	Shielded	Ferrite	5.0	5.0	3.0
D53LC Type A	10	1.77	0.090	Shielded	Ferrite	5.0	5.0	3.0
D53LC Type A	15	1.40	0.142	Shielded	Ferrite	5.0	5.0	3.0
D53LC Type A	22	1.15	0.208	Shielded	Ferrite	5.0	5.0	3.0
D75C	6.8	1.79	0.050	Shielded	Ferrite	7.6	7.6	5.1
D75C	10	1.63	0.055	Shielded	Ferrite	7.6	7.6	5.1
D75C	15	1.33	0.081	Shielded	Ferrite	7.6	7.6	5.1
D75C	22	1.09	0.115	Shielded	Ferrite	7.6	7.6	5.1
D104C	10	4.3	0.0265	Shielded	Ferrite	10.0	10.0	4.3
D104C	16	3.3	0.0492	Shielded	Ferrite	10.0	10.0	4.3
D104C	22	2.5	0.0265	Shielded	Ferrite	10.0	10.0	4.3
D10FL	10	2.26	0.051	Open	Ferrite	9.7	11.5	4.0
D10FL	15	2.00	0.066	Open	Ferrite	9.7	11.5	4.0
D10FL	22	1.83	0.100	Open	Ferrite	9.7	11.5	4.0
Coilcraft								
DO3308	10	2.4	0.030	Open	Ferrite	9.4	13.0	3.0
DO3308	15	2.0	0.040	Open	Ferrite	9.4	13.0	3.0
DO3308	22	1.6	0.050	Open	Ferrite	9.4	13.0	3.0
DO3316	10	3.8	0.030	Open	Ferrite	9.4	13.0	5.1
DO3316	15	3.0	0.040	Open	Ferrite	9.4	13.0	5.1
DO3316	22	2.6	0.050	Open	Ferrite	9.4	13.0	5.1

HWD63020Dx Demo Board Schematic

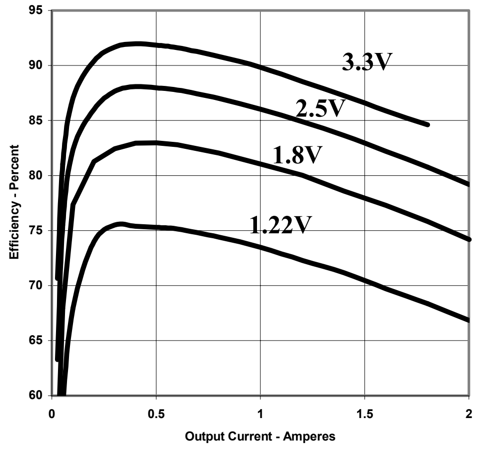
This board is laid out to accommodate most commonly used Inductors and Output Capacitors; and to be programmed for most standard Output Voltages. For the required Output voltage solder blob the appropriate J1-6 jumper.



Efficiency versus Output Current and Voltage. V_{IN}=10V



Efficiency versus Output Current and Voltage. V_{IN} = 5V



HWD63020Dx Demo Board BOM

Item	Quantity	Reference	Part
1	2	CN1	4 Pin Connector
		CN2	4 Pin Connector
2	1	Cb	10nF 0603
3	1	Cc	22nF 0603
4	1	Cca	100pF 0603
5	1	C1	10uF 25V 1210
6	1	C4	22uF 10V Y5V 1210
7	1	D1	B230/SM 2A 30V Schottky
8	1	L1	15uH
9	2	RC	10K 1%
		R1	10K 1%
10	1	R2a	2.32K 1%
11	1	R2b	4.75K 1%
12	1	R2c	10.5K 1%
13	1	R2d	16.9K 1%
14	1	R2e	30.9K 1%
15	1	U1	HWD63020Dx/SO8

Table VI. Recommended components for standard output voltages.

Vout	Jumper connection	L1 minimum	R_C
1.22V	J1	6.8uH	4.7K
1.5V	J2	6.8uH	4.7K
1.8V	J3	10uH	4.7K
2.5V	J4	10 uH	10K
3.3V	J5	15 uH	10K
5.0V	J6	22 uH	10K

Refer to the HWD63020Dx Datasheet's Table IV Inductor Selection Guide for choosing L1.

OUTLINE DIMENSIONS

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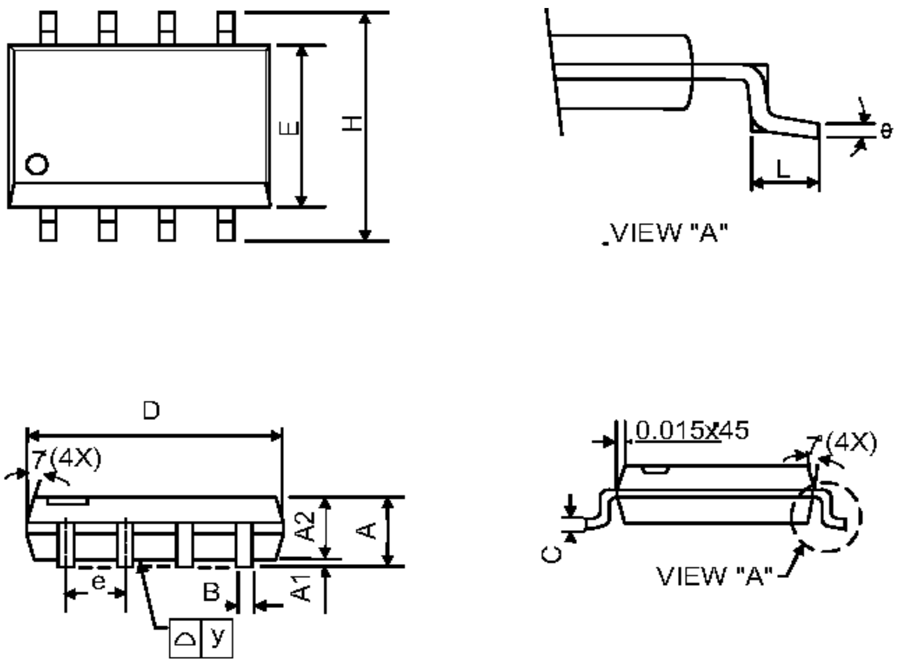

SYMBOLS	DIMENSION IN MILLIMETER (mm)			DIMENSION IN INCH (inch)		
	Min	Nom	Max	Min	Nom	Max
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	4.85	5.05	0.189	0.191	0.199
E	3.80	3.91	4.00	0.150	0.154	0.157
E	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
θ	0	-	8	0	-	8

Chengdu Sino Microelectronics System Co.,Ltd

(Http://www.csmsc.com)

Headquarters of CSMSC

Address: 2nd floor, Building D, Science & Technology Industrial Park, 11 Gaopeng Avenue, Chengdu High-Tech Zone,Chengdu City, Sichuan Province, P.R.China

PC: 610041

Tel: +86-28-8517-7737-230

Fax: +86-28-8517-5097

Beijing Office:

Address: Room 505, No. 6 Building, Zijin Garden, 68 Wanquanhe Rd., Haidian District, Beijing, P.R.China

PC: 100000

Tel: +86-10-8265-8662

Fax: +86-10-8265-8663

Shenzhen Office:

Address: Room 1015#, Building B, Zhongshen Garden, Caitian Rd., Futian District, Shenzhen, P.R.China

PC: 518000

Tel: +86-775-8299-5149
+86-775-8299-5147
+86-775-8299-6144

FAX:+86-775-8299-6142

Shanghai Office:

Address: Room C-603, High-Tech King World, Beijing East Rd. , Shanghai, P.R.China

PC: 200001

Tel: +86-21-5308-2272 ext. 210
+86-21-5308-2273 ext. 210

Fax: +86-21-5308-2863